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STB Takes microSPARC™-II to 85 and 100MHz

70MHz microSPARC-II Chipset Pricing Announced

MOUNTAIN VIEW, March 15, 1994 – SPARC Technology Business (STB) today announced sampling of high-end 85MHz and 100MHz microSPARC™-II RISC microprocessors. In addition, STB has announced pricing for a highly-integrated SPARC® solution consisting of a 70MHz microSPARC-II and the companion STP2000/2001 SBus combination-I/O chipset. Announced in October, the microSPARC-II – with over twice the performance of the original microSPARC processor – is a scalable "system on a chip" intended for low-cost, low-power systems.

The microSPARC-II integrates a SPARC V8 RISC processor, floating point unit, memory controller, memory management unit, cache, SBus controller, graphics bus support and phase-locked loop clock generator onto a single device. The new chip, implemented in a three-layer 0.5µ CMOS technology developed by Fujitsu Ltd. (Tokyo), improves on Sun's earlier microSPARC RISC processor in several significant ways.

microSPARC-II/microSPARC Feature Comparison

	microSPARC	microSPARC-II	improvement
cache	6KB	24B	4X
cache-refill bus	32 bits	64 bits	2X
clock frequency	50MHz	70-100MHz	1.4-2X
DRAM (maximum)	128MB	256MB	2X
performance	26 SPECint 92	51-67 SPECint 92	2X+
transistor count	800,000	2.4 million	3X
TLB	32 entries	64 entries	2X
write buffer	one entry	four entries	4X

- *more* -

Additional features found in microSPARC-II result in a number of key benefits, including:

- reduced power consumption through lower operating voltage (reduced from 5.0 volts), coupled with integrated power management circuitry
- 24 bit/pixel acceleration to video/graphics subsystems is provided by a high-bandwidth local bus interface
- improved logic schemes (such as branch folding) and other superscalar techniques
- SBus throughput is more than doubled through longer burst size and pipelined Direct Memory Access.

Highly-Integrated Support Logic

Just as the microSPARC-II captures several key components on a single IC, the companion STP2000/2001 SBus combination-I/O chipset integrates the power of a complete I/O subsystem in two logic devices. This Highly-Integrated Support Logic Circuitry (HISC) lets system designers develop microSPARC-II motherboards with only three CPU core cluster chips.

The STP2000/2001 chipset consists of two chips which integrate an entire I/O subsystem and utilize a single logical SBus slot. With the addition of memory, the microSPARC-II and STP2000/2001 chipset comprise a complete computer architecture.

STB offers the complete 70MHz microSPARC-II three-chip set (CPU and I/O ASICs) priced at $540 in 5K quantities.

SPARC Technology Business (STB), a division of Sun Microsystems, Inc., was formed in April 1993 to develop, design and distribute SPARC technologies and products worldwide. STB's portfolio includes microprocessors, chipsets, modules, boards, technology licenses, silicon and system design packages and consulting services. Currently, STB has more than 400 employees working in product development, engineering, marketing and international sales and support.

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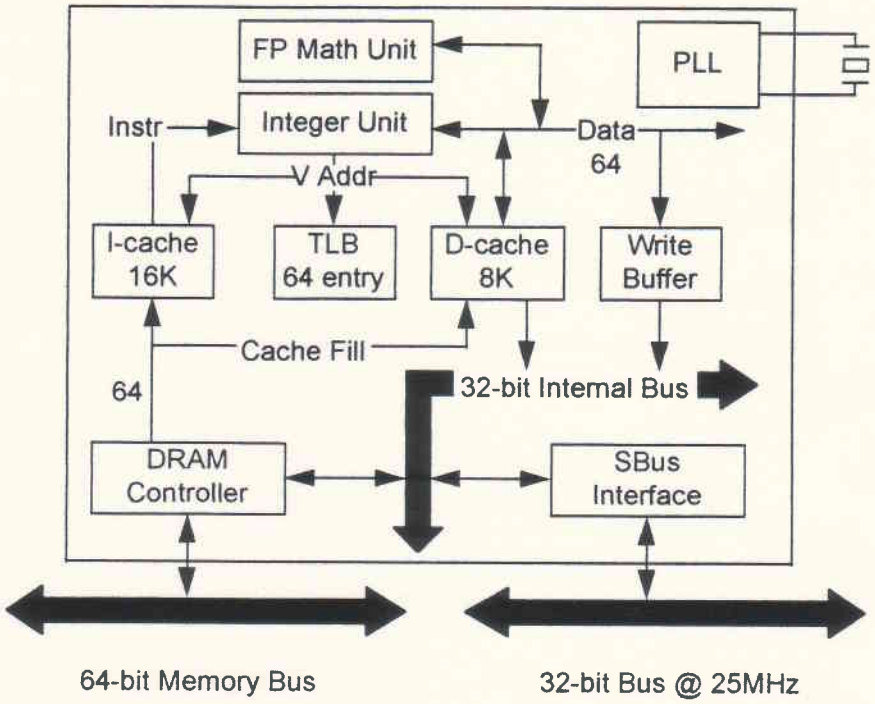
microSPARC-II CPU

DATASHEET



- SPARC V8 uniprocessor architecture
- On-chip Instruction and Data Caches
- IEEE 754 SPARC Floating Point Unit
- Combined SPARC Reference and I/O Memory Management Units
- DRAM interface
- IEEE SBus P1496 conformance
- IEEE 1149.1 JTAG conformance